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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,717	10/17/2005	Masakazu Sagawa	1113.44721X00	8398

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EXAMINER	
PERRY, ANTHONY T	
ART UNIT	**PAPER NUMBER**
2879	

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04/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,717	SAGAWA ET AL.	
	Examiner	Art Unit	
	ANTHONY T. PERRY	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusunoki et al. (JP 2001-084891).

Regarding claim 1, Kusunoki et al. disclose a cold cathode type flat panel display comprising: a first substrate (1) including thin-film type electron sources arranged in arrays, each of said thin-film type electron sources including a lower electrode (9), an upper electrode (13) and an electron acceleration layer (12) retained between said lower electrode and said upper electrode (13), each of said thin-film type electron sources emitting electrons from said upper electrode (13) in response to a voltage applied between said lower electrode (9) and said upper electrode (13); and a second substrate (110) including a fluorescent screen in which a plurality of phosphors (111,112,113) to be excited by said electrons emitted from said first substrate are arrayed; said cold cathode type flat panel display being characterized in that each of said arrays of said thin-film type electron sources includes a first interlayer insulation layer (14) and an upper electrode feeder wiring (15) serving as a power feed line to said upper electrode (13); and a second interlayer insulation layer (14) is provided between said first interlayer insulation layer (14) and said upper electrode feeder wiring (15) (for example, see Figs. 1(f) and 6).

Regarding claim 2, Kusunoki teaches that the lower electrode (9) is made of aluminum or an aluminum alloy; said electron acceleration layer (12) and said first interlayer insulation layer are anodic oxide films of said aluminum or aluminum alloy forming said lower electrode; and said second interlayer insulation layer (14) is made of an insulation film material which can be etched selectively with respect to said lower electrode and said anodic oxide films of said aluminum or aluminum alloy forming said lower electrode (9) (for example, see paragraphs 0013-0016).

Regarding claim 3, Kusunoki discloses a terminal portion of said second interlayer insulation layer (14) surrounding an electron acceleration region (12) has a normal dip shape (for example, see Figs. 1(f) and 6).

Regarding claim 4, Kusunoki discloses teaches the second interlayer insulation layer (14) has a structure of a plurality of layers; and said second interlayer insulation layer has a normal dip shape in a terminal portion thereof surrounding an electron emission region, said normal dip shape being formed using a difference in etching rate among said layers (for example, see Fig. 6 and paragraphs 0014-0015).

The Examiner notes that the claim limitation that "said normal dip shape being formed using a difference in etching rate among said layers" is drawn to a process of manufacturing which is incidental to the claimed apparatus. It is well established that a claimed apparatus cannot be distinguished over the prior art by a process limitation. Consequently, absent a showing of an unobvious difference between the claimed product and the prior art, the subject product-by-process claim limitation is not afforded patentable weight (see MPEP 2113). Therefore, it is the position of the examiner that it would have been obvious to one of ordinary

skill in the art that the dip shape disclosed by Kusunoki is at least a fully functional equivalent to the Applicant's claimed dip shape as evidenced by Kusunoki suggestion of all of the Applicant's claimed structural limitations.

Regarding claim 5, Kusunoki discloses a cold cathode type flat panel display comprising a substrate (1) and a fluorescent screen (111,112,113), said substrate including thin-film type electron sources arranged in arrays, each of said thin-film type electron sources including a lower electrode (9), an upper electrode (13) and an electron acceleration layer (12) retained between said lower electrode (9) and said upper electrode (13), each of said thin-film type electron sources emitting electrons from said upper electrode (13) in response to a voltage applied between said lower electrode (9) and said upper electrode (13); said cold cathode type flat panel display being characterized in that: each of said arrays of said thin-film type electron sources includes a first interlayer insulation layer (14), an upper electrode feeder wiring (15) serving as a power feed line to said upper electrode (13), and a second interlayer insulation layer (14) having an opening and put between said first interlayer insulation layer (14) and said upper electrode feeder wiring (15); and a region for emitting electrons is defined by a region of said opening of said second interlayer insulation layer (14) (for example, see Figs. 1(f) and 6)..

Regarding claim 6, Kusunoki teaches that the lower electrode (9) is made of aluminum or an aluminum alloy; said electron acceleration layer (12) and said first interlayer insulation layer are anodic oxide films of said aluminum or aluminum alloy forming said lower electrode; and said second interlayer insulation layer (14) is made of an insulation film material which can be etched selectively with respect to said lower electrode and said anodic oxide films of said

aluminum or aluminum alloy forming said lower electrode (9) (for example, see paragraphs 0013-0016).

Regarding claim 7, Kusunoki discloses a terminal portion of said second interlayer insulation layer (14) surrounding an electron acceleration region (12) has a normal dip shape (for example, see Figs. 1(f) and 6).

Regarding claims 8-9, Kusunoki discloses teaches the second interlayer insulation layer (14) has a structure of a plurality of layers; and said second interlayer insulation layer has a normal dip shape in a terminal portion thereof surrounding an electron emission region, said normal dip shape being formed using a difference in etching rate among said layers (for example, see Fig. 6 and paragraphs 0014-0015).

The Examiner notes that the claim limitation that "said normal dip shape being formed using a difference in etching rate among said layers" is drawn to a process of manufacturing which is incidental to the claimed apparatus. It is well established that a claimed apparatus cannot be distinguished over the prior art by a process limitation. Consequently, absent a showing of an unobvious difference between the claimed product and the prior art, the subject product-by-process claim limitation is not afforded patentable weight (see MPEP 2113). Therefore, it is the position of the examiner that it would have been obvious to one of ordinary skill in the art that the dip shape disclosed by Kusunoki is at least a fully functional equivalent to the Applicant's claimed dip shape as evidenced by Kusunoki suggestion of all of the Applicant's claimed structural limitations.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Anthony Perry* whose telephone number is **(571) 272-2459**. The examiner can normally be reached between the hours of 9:00AM to 5:30PM Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. **The fax phone number for this Group is (571) 273-8300.**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Anthony Perry/

Anthony Perry
Patent Examiner
Art Unit 2879
March 28, 2008

/Nimeshkumar Patel/

Supervisory Patent Examiner, Art Unit 2879